JEDEC/IPC
JOINT PUBLICATION

Current Tin Whiskers Theory and Mitigation Practices Guideline

JP002

MARCH 2006

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION
IPC ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES®

NOTICE

JEDEC and IPC Standards and Publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for his particular need. Existence of such Standards and Publications shall not in any respect preclude any member or nonmember of JEDEC or IPC from manufacturing or selling products not conforming to such Standards and Publications, nor shall the existence of such Standards and Publications preclude their voluntary use by those other than JEDEC and IPC members, whether the standard is to be used either domestically or internationally.

Recommended Standards and Publications are adopted by JEDEC and IPC without regard to whether their adoption may involve patents on articles, materials, or processes. By such action, JEDEC and IPC do not assume any liability to any patent owner, nor do they assume any obligation whatever to parties adopting the Recommended Standard or Publication. Users are also wholly responsible for protecting themselves against all claims of liabilities for patent infringement.

The material in this joint standard was developed by the
JEDEC JC-14.1 Committee on Reliability Test Methods for Packaged Devices
and the IPC Tin Whiskers Guideline Task Group (5-23e).

For Technical Information Contact:

JEDEC Solid State Technology Association
2500 Wilson Boulevard, Suite 220
Arlington, VA 22201
Phone (703) 907-7500
Fax (703) 907-7583

IPC
3000 Lakeside Drive, Suite 309S
Bannockburn, Illinois 60015-1219
Tel (847) 615-7100
Fax (847) 615-7105

PLEASE!

DON'T VIOLATE
THE
LAW!

CURRENT TIN WHISKER THEORY AND MITIGATION PRACTICES GUIDELINE

Foreword

This publication provides guidance in understanding the prevalent tin whisker formation theories, driving forces and mitigation practices used to minimize tin whisker formation. This publication serves as a source of background information for JESD22-A121, *Measuring Whisker Growth on Tin and Tin Alloy Surface Finishes* and JESD201, *Environmental Acceptance Requirements For Tin Whisker Susceptibility of Tin and Tin Alloy Surface Finishes*.

Introduction

Sn whiskers have been an industrial concern and interesting problem for many years. They are known to cause short circuits in fine-pitch pretinned electrical components [1]. Sn whiskers grow by the addition of material at their base not at their tip (i.e., they grow out of the substrate) [2]. They can grow from as-formed electrodeposits, vapor deposited material [3], and intentionally deformed coatings of Sn [4]. Similar whiskers are observed in Cd, In, and Zn [5]. Whiskers appear to be a local response to the existence of residual stress. Compressive residual or external stress is usually considered a precondition for whisker growth [4]. Annealing or melting (reflow in solder terminology) may mitigate the growth for an undetermined period of time. In 1959, Pb additions of a few percent to Sn electroplate were found to greatly reduce the tendency to form whiskers [6] and interest in the subject waned. Legislation that will restrict the use of lead in electronic products sold in the European Union, due to be in effect on July 1, 2006, has led many electronic component suppliers to propose the removal of Pb from tin-lead plating, leaving essentially pure Sn. This approach is the most convenient and the least costly lead-elimination strategy for the majority of component manufacturers. However, for the high-reliability user community, the pure tin strategy presents reliability risks due to the whisker forming tendencies of pure tin and tin alloy plating.

This publication discusses the current tin whisker history, theories and driving forces behind tin whisker formation and potential mitigation practices for various applications. It should be noted that for certain applications with special needs (e.g., military or aerospace), the Sn mitigation methods contained in this document may not be sufficient due to additional performance requirements [7].

CURRENT TIN WHISKER THEORY AND MITIGATION PRACTICES GUIDELINE

(From JEDEC Board Ballot JCB-05-143, Formulated under the cognizance of the JC-14.1 Subcommittee on Reliability Test methods for packaged Devices in conjunction with the IPC Tin Whiskers Guideline Task Group (5-23e).)

1 Scope

This document will provide insight into the theory behind tin whisker formation as it is known today and, based on this knowledge, potential mitigation practices that may delay the onset of, or prevent tin whisker formation. The potential effectiveness of various mitigation practices will also be briefly discussed. References behind each of the theories and mitigation practices are provided.

2 Terms and definitions

For the purposes of this publication, the following terms and definitions apply.

whisker: A spontaneous columnar or cylindrical filament, usually of monocrystalline metal, emanating from the surface of a finish. (See Annex C for example pictures of tin whiskers.)

whisker growth: Measurable changes in whisker length and/ or whisker density.

tin whisker mitigation practice: Process(es) performed during the manufacture of a component to reduce the propensity for tin whisker growth by minimizing the surface finish internal compressive stress.

matte tin: A tin film with lower internal stresses and larger grain sizes typically of 1µm or greater and carbon content less than 0.050% [8].

bright tin: A tin film with higher internal stresses and smaller grain size of 0.5 µm to 0.8 µm and carbon content of 0.2% to 1.0% [8].

Underlay: A plated barrier layers between the base metal and the tin finish.

3 History of tin whiskers

A metallic whisker is generally a single crystalline filamentary surface eruption from a metal surface, though polycrystalline filamentary surface eruptions have been observed [9,10]. Whiskers are usually found on relatively thin, 0.5 µm to 50 µm , metal films that have been deposited onto a substrate material. A typical whisker is one to five µm in diameter and between 1 µm and 500 µm long [8]. Whiskers can be straight, kinked, or even curved, see Annex C. Metallic film deposits have also shown other types of eruptions that are quite different in appearance from the whisker eruption. These eruptions are referred to in the literature as flowers, extrusions, and volcanoes. They have not been of as much general interest as the much-longer whisker eruptions.

3 History of tin whiskers (cont'd)

Metallic whisker formation first became of widespread interest to the scientific community immediately after WWII. In 1948, the Bell Telephone Corporation experienced failures on channel filters used to maintain frequency bands in multi-channel telephone transmission lines. Bell Laboratories quickly initiated a series of long-term investigations into the general topic of whisker formation, the results of which were first reported in 1951 by K.G. Compton, A. Mendizza, and S.M. Arnold [11]. This Bell Laboratories work established that whisker formation occurred spontaneously, on cadmium (Cd), zinc (Zn), and tin (Sn) electroplating. The Bell Lab experiments studied a variety of substrate materials including copper (Cu), copper alloys, steels, and nonmetallic substrates.

An excellent annotated bibliography of tin whisker history and references is provided [8] that include a comprehensive listing of articles published through Dec. 31, 2004.

One reason that the problem of tin whiskers has not been solved is the lack of appropriate analytical tools to study the basic structure of the Sn film. Only in recent years have tools like Focused Ion Beam (FIB), Synchrotron X-Ray Diffraction, and Electron Back Scattering Beam (EBSD) become available for researchers to use in investigating this problem. As data from these tools becomes available, the industry may get a better understanding of tin whisker formation and the reasons they occur [12].

Other reasons that the whisker problem has not been solved are: 1) all of the variables that effect whisker growth are not known, 2) variables known or suspected of affecting whisker growth are not always reported when data is published, 3) Pb has been used as a mitigation method for whisker growth for decades, 4) current test methods cannot correlate whisker growth in test conditions to field conditions, and 5) as such, test results cannot be used to predict whisker growth in other environments or longer durations.

4 Discussion of and theory behind whisker formation

The following information represents the generally accepted knowledge on the prevailing theory of tin whisker formation available at this time. It is intended to aid suppliers in understanding whisker formation and how tin whiskers formation might be minimized or delayed on products. Many of the mitigation methods described in this document are based on interrupting the development of compressive stress in the tin layer.

The lead-frame material or substrate has a major impact on whisker formation, and as such, has been one of the factors causing confusion and inhibiting consistent conclusions from being formed. It should be noted that the information provided in this publication refers to 100% Sn plating on a copper-based lead frame materials, unless otherwise specified.

Another area for confusion in interpreting results has been the use of matte versus bright tin. In general, matte tin films are less prone to whisker formation and growth than so-called bright tin films. Many current suppliers claim that a proprietary version of matte tin is whisker-free, but these claims may be premature and should be considered carefully before use. This document refers only to matte tin finishes unless otherwise noted.

In reporting and analyzing results, all pertinent information should be noted including, but not limited to, type of tin used, lead frame material, and any underlay material.

4 Discussion of and theory behind whisker formation (cont'd)

4.1 Primary cause of whisker formation

The driving force behind tin whisker formation is stress in the Sn film [13]. Stress may come from the as-plated film with its associated texture [14,15], intermetallic formation or mechanical means, such as bending, forming, thermo-mechanical stresses (CTE mismatch induced), or possibly oxygen diffusion and/or oxide formation on the surface. The corrosion of Sn is another possible source for the stress in the Sn finish [9,16]. Compressive stresses are fundamental to all whisker formation and provide a driving force for the creation of whiskers.

In many cases the driving force behind a reaction, such as a compressive stress, is eliminated or reduced by diffusion-based relaxation mechanisms. These mechanisms can slow or stop the reaction. However, there are some cases where the driving force is not relieved by diffusion or other solid state mechanisms. In addition, it is possible that the driving force can be continuously regenerated or renewed. In these cases the driving force remains active. Intermetallic formation, oxide reactions at the film surface, temperature cycling, and certain kinds of constant mechanical clamping forces are all examples of conditions where the compressive stress is continually regenerated or is undiminished by solid state mechanisms. However, stress is a necessary but not solely sufficient condition for whisker formation. It appears that there has to be a specific type of crystalline microstructure required that is favorable to a localized surface eruption or whisker [16, 17]. The variation in whisker "incubation times", which range from minutes to decades, is believed to be due to the mechanisms involved in nucleating these specialized crystalline microstructures and/or the time required to build up sufficient compressive stress in the Sn films to start whisker formation [18]. If the film stress levels are maintained at a high enough compressive level for a long enough period of time, there will be a very high likelihood of a whisker growth event as a means of further relaxing the stress levels within the film beyond the extent affected by simple diffusion.

It is believed that one of the prime causes of stress that may result in whisker formation, as seen in testing, is the irregular growth of the Cu_6Sn_5 intermetallic, when Sn is plated on Cu based substrates, which occurs rather quickly under room ambient conditions [19]. The irregular growth of intermetallic compounds is also referred to as a chemical reaction.

Another source of stress in electronic components is CTE mismatch induced stresses [20]. These are particularly significant when the substrate material has a low CTE, such as Alloy 42.

In addition to stress associated with component material mismatches, any mechanical stresses associated with the product may play a role in whisker formation. This could include stress in the Sn layer due to the assembly loading conditions associated with specific product. More research is needed in this area to better understand the interaction of other mechanical stresses and whisker formation.

4.1 Primary cause of whisker formation (cont'd)

4.1.1 Effect of Cu_6Sn_5 formation by diffusion

Cu_6Sn_5 forms in the Sn layer on Sn plated Cu surfaces at room ambient and is dominant at temperatures below 60 °C, creating compressive stress in the Sn layer. The stress generated by the formation of Cu_6Sn_5 is thought to be caused by two contributing factors:

a) At any temperature, such as ambient, the diffusion of Cu into Sn proceeds through grain boundary diffusion and forms intermetallics. At room temperature the primary intermetallic is Cu_6Sn_5 and grain boundary diffusion is significantly faster than bulk diffusion. This results in irregular growth of Cu_6Sn_5 in the grain boundaries of the Sn. However, at some elevated temperature above room ambient, generally about 2/3 of the absolute melt temperature, bulk diffusion becomes increasingly significant, see Figure 1.

b) There are two schools of thought for the formation of compressive stresses in the Sn film in and around the Cu-Sn intermetallic and the Sn(Cu-Sn-to-Sn interface). 1) If six parts of Cu are mixed with five parts of Sn, the resultant Cu_6Sn_5 has a larger molar volume than the Sn and Cu from which it was formed; this in itself would lead to compressive stresses at the Cu-Sn-to-Sn interface. 2) Alternatively, if one considers Cu to infiltrate the Sn lattice sites in the Sn film leaving behind open space in the underlying Cu, then the overall reaction will lead to an increase in volume in and around the Cu-Sn-to-Sn interface. This also acts as a compressive layer of Sn. Furthermore, at lower temperatures the growth of the Cu_6Sn_5 phase is dominated by grain boundary diffusion. As such the interface between the Sn grains and the Cu_6Sn_5 phase is non-planar. This can also act to increase the localized compressive stresses in the Sn film [21]

Storage at 5 °C greatly reduces, but does not stop, intermetallic compound (IMC) formation. Although this has not been explored in depth, it may be a way to store whisker test samples for future comparisons. Oxide growth follows similar kinetics and would be similarly affected by low temperature storage. Recent experience has also shown that Sn pest does not seem to be a problem with today's commercial plating operations [22].

As stated earlier, at higher temperatures, the primary diffusion mechanism changes from grain boundary diffusion to bulk diffusion. This results in changes in the intermetallic layer:

1) Somewhere above 60 °C, exact temperature not established, Cu_3Sn will form from the Cu_6Sn_5 and is found between the Cu_6Sn_5 and Cu layer. Cu_3Sn has a lower molar volume and will not add to stress in the Sn layer.

2) Due to bulk diffusion at higher temperatures a more regular intermetallic double layer (Cu_3Sn and Cu_6Sn_5) will form. This forms the basis for a mitigation strategy of heat treating at temperatures of 150 °C as is further discussed in section 5.4.3

4.1 Primary cause of whisker formation (cont'd)

4.1.1 Effect of Cu_6Sn_5 formation by diffusion (cont'd)

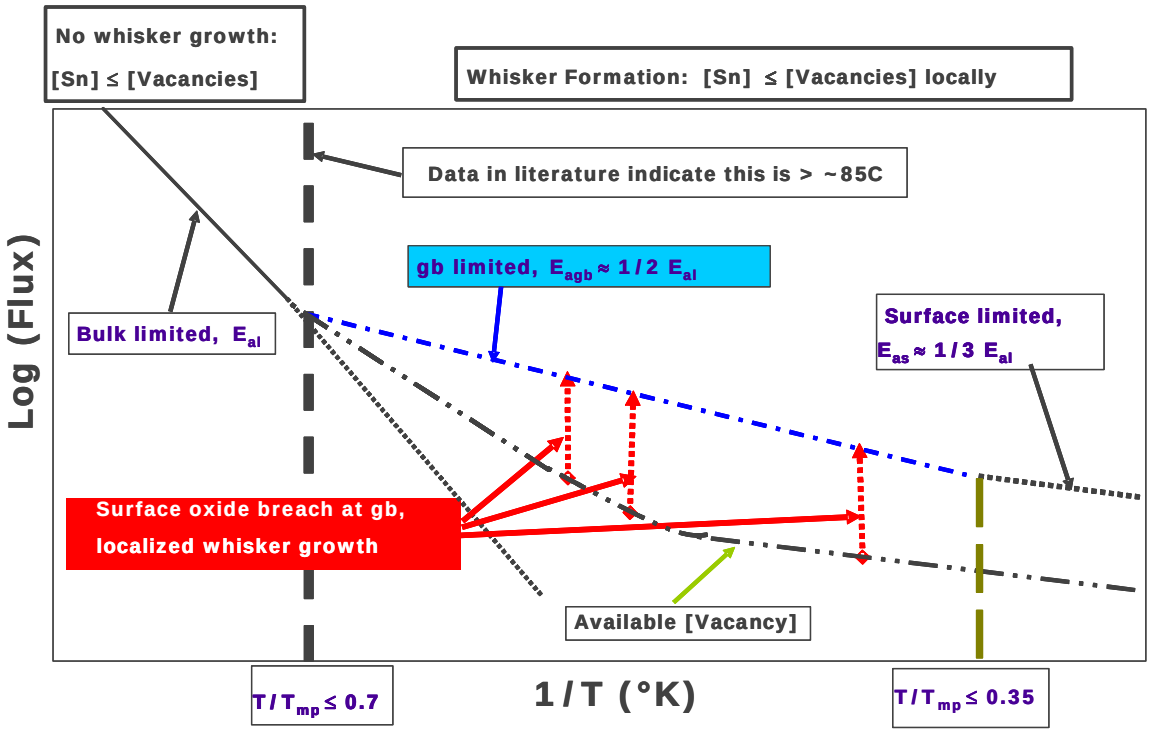


Figure 1 — Grain Boundary vs. Bulk Diffusion

Figure 1 shows a schematic representation of the temperature ranges where the dominant diffusion mechanism transitions occur in typical polycrystalline materials, namely surface, grain boundary, and lattice (bulk) diffusion. Note that both the slope, activation energy (E_a), and the intercept (D_O), significantly differ for the three different diffusion mechanisms. Stress relaxation in typical polycrystalline materials occurs via diffusion. In the temperature range where Sn whiskers typically occur, 85 °C ≥ T ≥ -55 °C, the predominant diffusion mechanism is expected to be grain boundary diffusion. Therefore, it is assumed that Sn whisker formation is controlled by grain boundary diffusion. However, because the system is pinned, (i.e., grain growth either occurs very slowly or not at all in the temperature range where Sn whiskers are typically found to grow) the diffusion rate can be considered to be limited by the available vacancy flux, such that grain boundary diffusion is also controlled by vacancy flux in this system. Localized breaches in the surface oxides will for some finite period of time (the time period is defined by the rate of re-oxidation of the surface of the Sn film were the oxide was breached), provide an infinite source of vacancies from the ambient air that can increase the available flux of vacancies. At this location, the rate of grain boundary diffusion can approach the intrinsic (non-pinned) rate. However, because all of the grain boundaries are pinned, the excess Sn that is present in the system from things such as compressive stresses can only be reduced via grain boundary diffusion along the grain boundaries that are in the vicinity of the breach. If the grain boundary has a nucleation site on it, then a whisker can begin to nucleate and grow at that location. Over time the Sn nuclei grow forming whiskers.

4.1 Primary cause of whisker formation (cont'd)

4.1.1 Effect of Cu_6Sn_5 formation by diffusion (cont'd)

At temperatures greater than ≅85 °C or T/Tmp ≥ 0.7 (actual temperature/melting point temperature), bulk diffusion begins to dominate. When this occurs, the thermally generated vacancy concentration is sufficient to un-pin the system. Thus the excess stresses in the film will then be reduced by more global related mechanisms such as re-crystallization and grain boundary growth, therefore effectively dominating the more localized stress reduction mechanisms that drive Sn whisker formation and growth.

An irregular IMC formation will create more stress in "thin" (2-3 μm) layers of Sn than in thicker (7 μm or greater) layers. The thicker layer has a greater volume and as such an overall lower stress in the Sn film resulting in longer times needed to initiate whiskers.

Stress alone, though, may not be enough to initiate whisker formation. An initiation event is required. Whiskers are generally localized to particular grains in the Sn layer. It is speculated this is because they have low-angle grain boundaries with their adjacent as-deposited grains, and the grain boundaries are oblique with respect to the film surface [18, 23].

4.1.2 Impurities

It appears that impurities in the plating bath and other defects may also enhance the possibility of whisker formation. It is not understood which impurities are the culprits and the levels to which they should be controlled. But copper and carbon appear to be impurities that make the tin film stress increasingly compressive [24].

4.1.3 Oxide formation and humidity

The role of oxide formation is not well understood. Humidity apparently introduces stresses from the diffusion of oxygen downward from the surface [25]. By comparison, intermetallics introduce stresses from the substrate interface towards the surface.

High humidity will affect the thickness of the oxide film on the Sn layer leading to compressive stress [17]. Impurities or defects in the oxide film may also contribute to whisker formation [26]. High humidity might lead to corrosion, which could introduce additional stress see clause 4.1.4 [16]. The relation to actual field life of these test conditions is unknown. Serious consideration should be given to storage conditions. Additionally, the high humidity may affect surface diffusion rates of Sn.

4.1.4 Condensation and corrosion

Condensed moisture exposure, either by water condensation during high-temperature humidity testing or via water droplet exposure, can lead to corrosion assisted whisker growth [27]. Excessive localized surface corrosion can produce non-uniform oxide growth that imposes additional differential stress states on the Sn film. The combination of condensed moisture and higher temperatures has been shown to produce either localized clusters of whiskers or accelerated growth of an individual whisker. Often identified as lead termination "black spot corrosion", whiskers found to nucleate in the corroded regions will continue to grow even after removal of the condensed moisture. Corrosion has been identified as a confounding factor in extended duration, high humidity testing. See JESD 201 for a discussion of and disposition of whiskers found on corroded leads. Impurity segregation in conjunction with the evaporation and condensation of water could also lead to enhanced whisker growth effects.

4.2 Incubation time

The incubation time before whiskers form has been very unpredictable. Under high stress conditions, whiskers have been grown very rapidly. In other cases, years have passed before whisker growth has been seen at all. This may be due to the requirements for a recrystallization event to occur that creates an appropriate whisker grain, or whisker growth may be delayed due the length of time required to build sufficient stress to start the whisker formation process.

5 Finish and substrate considerations and mitigation methods

The finish and substrate mitigation methods listed in this publication are based on current knowledge and beliefs. They are not listed in any order of preference or relative effectiveness. Selection of a method should be based on the product and application specifics. Appropriate verification testing should be performed to determine effectiveness in the given application.

Mitigation refers to processes or materials that greatly enhance resistance to whisker formation for tin-based films, but do not necessarily prevent their ultimate formation. Since compressive stresses are thought to be fundamental to whisker formation, it would follow that mitigation approaches would somehow alter the stress state within the tin. Underlays, alloying, plating chemistry, and heat treatment all have an effect on the stress state of the tin and encompass the variety of commercially available mitigation methods.

Compressive stresses may be generated in the tin film in a number of ways. These stresses may be due, but not limited to:

a) intermetallic growth at the tin-substrate interface (Section 4.1.1).

b) a “uniform” surface oxide film which may create localized surface compression in the tin [28], also see Section 4.1.

c) the expansion of byproducts created by “gross” corrosion within the tin (e.g., “black spot corrosion”) [16]

d) oxidation penetrating from the surface into the Sn matrix, primarily along the grain boundaries, thus creating what may be envisioned as a “wedge” of expanding oxide by-products.

To date, whisker experimentation has been very inconsistent relative to growth rates, incubation times, and many other parameters. Nevertheless, certain whisker mitigation guidelines have been endorsed by various suppliers and users. It is important to understand that the various mitigation practices and techniques discussed in this publication are not always effective in reducing tin whiskers and should not be construed as whisker prevention methods, but rather as whisker risk reduction methods. It should also be noted that some mitigation methods in this document only address one form of stress generation. Since there may be multiple sources of stress in the Sn film, a given mitigation practice may not be sufficient to prevent tin whisker formation. To this end, a user must be able to evaluate the whisker growth over their products life expectancy at field conditions to be confident in the effectiveness of the mitigation method employed.

5 Finish and substrate considerations and mitigation methods (cont'd)

Other material sets and combinations can be considered if good technical arguments can be made regarding their effectiveness in the reduction of tin whiskers, and are backed up with tin whisker test data. The whisker test procedures used by the product supplier should also be specified.

The industry continues to work on a test method designed to quickly indicate a deposit's susceptibility to whisker growth. Any mitigation practice should be used with the understanding that the responsibilities to verify the impact of potential whisker growth on a system's long term reliability is the end users, see JESD201.

5.1 Non-tin plating

Non-tin plating, such as Nickel/Palladium/Gold, Nickel/Gold or Nickel/Palladium, do not have Sn whisker problems and should be considered for lead-frame applications. This plating has more than a ten year history of field use, 1992-to present [29]. Non-tin plating, however, does have other potential issues, including adhesion to mold compounds that need to be evaluated prior to product conversion.

5.2 Tin plating alloys

5.2.1 Addition of Lead (Pb)

Sn/Pb plating with >3% Pb [30] has been the industry accepted finish for over 50 years and has been shown to mitigate Sn whisker formation [31]. As such, it has become the standard used when comparing and evaluating Sn whisker mitigation practices. Adding lead (Pb) to tin (Sn) plating, though, is no longer a viable strategy for most products after July 1, 2006. This is due to pending European Union, US States, and Chinese regulations. It should be noted that even the use of Pb is not a 100% guarantee against the formation of whiskers.

5.2.2 Tin bismuth alloy finishes

Bismuth may aid in suppressing whisker growth, when added to tin in amounts of 2-4% by weight [32, 33, 34]. With lead/free solder, tin-bismuth is a viable candidate for component finishes. Tin/bismuth alloy finishes are controversial when used in conjunction with eutectic tin/lead solder [35, 36]. With eutectic tin/lead solder, it will be necessary to control the bismuth content of the finish between 3-5% so as to have enough bismuth to suppress whisker formation without getting into the compositional range of the low melting point ternary eutectic. The ternary eutectic is formed between tin/lead/bismuth with a melting point at 96 ^{o}C. However, it is not thermodynamically possible to form this ternary eutectic with small (1-5% by weight) additions of Bi to Sn finishes when soldered with Sn/Pb. There is a ternary tin/lead/bismuth peritectic that is thermodynamically viable for small additions of Bi and this peritectic has a melting point of 135 ^{o}C. In addition, keeping the Bi content low is required to retain solderability of formed leads.

5.2.3 Plated tin silver

Plated SnAg (2-4% Ag) alloys in limited testing have shown promise in reducing tin whisker growth [34].

5.3 Underlay materials

Underlays may be effective in mitigating formation and growth if the compressive stress-inducing mechanism originates at the tin-substrate interface.

5.3.1 Nickel

The growth rate of tin-nickel intermetallics is much lower than that of SnCu intermetallics. Sn diffuses into Ni [8,37], forming Ni_3Sn_4. As a result, the Sn layer tends to see a tensile stress due to a high vacancy or void concentration. So, adding a nickel (Ni) underlay between tin plating and a copper (Cu) base metal may mitigate whisker formation by forming a barrier to Cu diffusion into the Sn. The thickness, porosity and ductility of the nickel plating are very important to ensure an effective barrier layer for the copper that will not crack during lead forming. A minimum porosity-free layer thickness of 0.5µm has been shown to mitigate the growth of Sn-whiskers for devices subjected to Pb-free reflow assembly conditions [38]. This thickness has been shown to ensure that the nickel is not fully converted and consumed to IMC after 3x 260 °C reflows and that the nickel layer is sufficiently ductile and will not crack during a subsequent lead forming operation [39].

A Ni underlayer would presumably not be beneficial in conditions where the compressive stress-inducing mechanisms originate at the tin surface or within the tin matrix itself.

Ni does not prevent the corrosion and oxidation of Sn in a high humidity environment.

Furthermore, a Ni underlayer may not solve the stress generated due to CTE mismatch, e.g., where the substrate is ceramic.

5.3.2 Silver

Adding a silver (Ag) underlayer between tin plating and copper (Cu) base metal has been proposed as a method to mitigate whisker formation, similar to Ni as noted above [40]. Components using silver under plating should have a minimum silver thickness of 2µm. However, there is limited whisker test data supporting the effectiveness of the Ag underlayer as whisker mitigation. Further investigation of the effectiveness of this technique is encouraged.

5.4 Heat treatments

Heat treatments may be subcategorized as annealing, fusing, and reflow. Annealing is a heating and cooling process typically intended to soften metals and make them less brittle. Fusing and reflow are similar in that both melt and resolidify tin plating under relatively slow cooling conditions.

5.4.1 Fusing tin plating

Fusing tin (Sn) plating shortly after plating may mitigate whisker formation [41]. Fusing is a reflowing operation usually done by dipping the tin-plated surfaces into a hot oil bath. Fused tin has shown an excellent field history [30]. If intermetallics form, see section 5.4.3, this may reduce the fusing effectiveness. Geometry effects must be considered. These factors may result in thinning of the Sn plating during fusing or reflow due to lead shape or propensity to be affected by whiskers due to lead pitch..

5.4 Heat treatments (cont'd)

5.4.2 Reflow in printed circuit board assembly process

Contrary to clause 5.4.1, fusing, done as part of the printed circuit board assembly process, has not been shown to be an effective mitigation practice. In a simulated reflow process without flux, there have been some cases where an increased growth of whiskers was observed. [42,43]. Future studies, where components are actually joined to the printed circuit board, are in progress to see what effect the assembly with solder has on whisker formation.

5.4.3 Annealing matte tin

In order to mitigate the whisker growth caused by irregular intermetallic growth, a heat treatment step of 1 hour at 150 °C for Cu based leadframes can be applied directly after plating, as explained in the following publications [14, 37, 40, 44]. This should be performed within 24 hours of plating to be effective.

This heat treatment step affects the Sn layer in several ways, see Figure 2-3:

1. Due to the bulk diffusion at this increased temperature a much more regular and continuous intermetallic layer will form, consisting of Cu_3Sn and Cu_6Sn_5, resulting in less compressive stress [37, 40, 44].

2. The grain boundaries of the Sn will shift, resulting in larger grains and less grain boundaries [40].

3. The more regular intermetallic layer will result in a continuous diffusion barrier for further growth of the Cu_6Sn_5 intermetallic, slowing further irregular growth by grain boundary diffusion at ambient conditions [44].

4. The post bake step can have an annealing effect, reducing the stress in the plating and reducing imperfections in the lattice of the Sn [14, 16].

This step is performed directly after plating, since the intermetallic grows under ambient conditions through grain boundary diffusion to several micrometers in the grain boundaries within one week after plating. The intermetallic layer generated by the postbake procedure is about 1 µm thick.

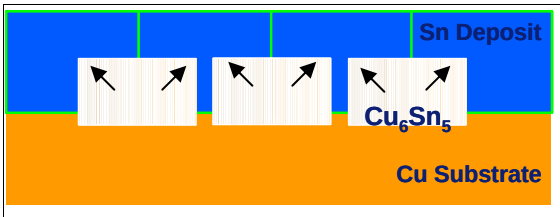


Figure 2 — Schematic drawing showing Cu_6Sn_5 growth in the grain boundaries at lower temperatures, resulting in irregular intermetallics.

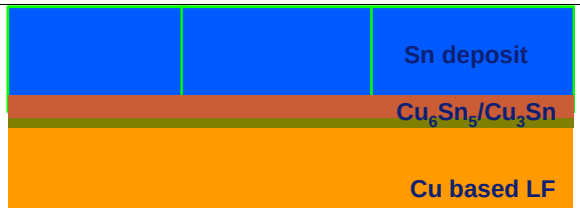


Figure 3 — Schematic drawing showing a regular double layer of Cu_3Sn/Cu_6Sn_5 through bulk diffusion after postbake.

5.5 Hot dip tin

Hot dip tin is a molten tin bath process that is intended for electronic components. It has primarily been used for structural steel parts, connectors and devices, such as relays, but not for leadframe components. Hot dipping with $SnAg_4$ or SnAgCu, is generally, an effective mitigation practice [46] and considered whisker free. However, there is evidence that when pure tin is used, this mitigation process may not be effective [46].

5.6 Thicker tin finish

Industry data indicates that thicker tin finishes show a lower propensity for tin whiskers and/or a greater incubation time before tin whiskers occur. It is recommended that the tin thickness for components without a nickel or silver underlayer be 7 µm minimum with 10 µm nominal [37,47,48]. When a nickel or silver underlayer plating is used, the minimum tin thickness should be of appropriate thickness to ensure component solderability over the intended shelf life and to prevent complete consumption of Ni in the intermetallic Ni/Sn phase.

5.7 Chemical etching copper alloys

Surface chemical etching prior to plating of copper based alloys in limited testing has shown promise in reducing tin whisker growth when the etching depth is in the range of 3 to 4 µm [19]. Further investigation of this technique, as a possible tin whisker mitigation practice, is needed.

5.8 Conformal coatings

The use of conformal coatings on a circuit board assembly has been shown to reduce the electrical shorting risks from whiskers [49,50]. Thicker coatings (≥ 3.9 mils) have been shown to prevent or delay whisker penetration while thinner coatings act as a dielectric layer for whiskers that may break off in an assembly. The use of conformal coating could be used in conjunction with other mitigation methods previously discussed. Conformal coatings also reduce the corrosion of Sn. There is an opportunity for more study in this area and the mitigation results will vary with the specifics of the assembly and its sensitivity to whisker problems.

5.9 Finish and surface considerations

5.9.1 Tensile stress tin films

The macro stress level of the tin deposit has an impact on tin whisker growth. Tin deposits that have tensile stress as plated and remain tensile with aging are preferred, see 4.1. Tin deposits that are compressive during service life are not preferred, see clause 4.1.

5.9.2 Effect of bias voltage

The extent and impact of bias is yet to be fully understood [51]. To date, there is no concrete evidence to show that bias voltage and/or current flow have an influence on Matte Sn [52]. In limited testing thus far, however, bias voltage has been shown to have an impact on tin whisker growth for bright Sn finishes [53].

5.9 Finish and surface considerations (cont'd)

5.9.3 Alloy 42 Leadframes:

Alloy 42 is an alloy of iron and nickel (42%), and under ambient conditions there appear to be few instances of whisker formation without irregularities (e.g. burrs, sharp edges) in the substrate given a well-controlled Sn plating process. Whisker growth is reported on thermal cycle testing, presumably due to the large CTE mismatch between alloy 42 and Sn.

Alternative lead plating for Alloy 42 are low porosity NiPdAu and Sn(1-4%)Bi plating (see above for whisker propensity). It should be noted that due to the large difference in electrochemical potential between Fe and Pd, there is a propensity for corrosion and this option should be verified appropriately. However, in accelerated thermal cycling tests with SnBi finishes on Alloy 42 lead-frames soldered with SnPb solder, the solder joint reliability has shown reductions ranging from approximately 15% [54] to more than 50% [55]. Industry data [56] has demonstrated that Alloy 42 component lead material can induce solder joint integrity degradation in accelerated stress testing due to printed wiring assembly to Alloy 42 lead material coefficient of thermal expansion (CTE) mismatch.

5.9.4 Tin copper alloys

Tin-copper alloys are not satisfactory finishes because copper enhances whisker formation and growth when included as an alloying element in tin plating [24].

5.10 Printed Circuit Board (PCB) and other component finishes

5.10.1 Immersion tin

Immersion tin is a chemical displacement process that results in a relatively thin (<40 micro-inches or 1 μm) and stress free tin film. Immersion tin's primary purpose as a surface finish for PCB applications, is solderability protection for the underlying copper basis metal.

As previously mentioned above, a potentially significant source for whisker formation are stresses induced from the formation of Cu_6Sn_5 intermetallic compounds (IMCs). While whisker formation is a concern, the primary concern is migration of the IMCs through the deposit and subsequent oxidation at the surface, thus rendering the deposit non-solderable. To this end it is imperative that the specification for a minimum deposit thickness of 1 μm be recommended. The thicker deposit improves shelf life, as a significant layer through which the IMCs must travel before solderability is impaired. [57]

The use of annealing procedures of 150 °C for 1 hour is not practical for printed circuit boards due to the potential negative impact of this temperature on warp & twist characteristics.

Whiskers have been grown on immersion tin conductive features To date, these whiskers have appeared at ambient conditions with time and not as a result of exposure to heat, vacuum, pressure, humidity or bias voltage [57]. This would seem to indicate that the primary source is Cu_6Sn_5 migration stress. Whisker length has been reported to be significant in vias, with lengths measured at 150 μm, see Figure 4. Whiskers of much smaller length have been recorded growing off the edge of surface mount (SMT) component pads, as well [57].

5.10 Printed Circuit Board (PCB) and other component finishes (cont'd)

5.10.1 Immersion tin (cont'd)

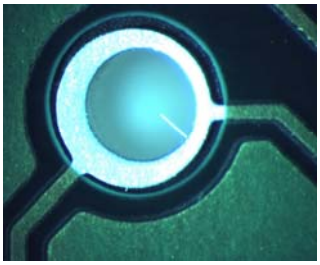


Figure 4 — Whisker in an Immersion Tin Plated 0.46 mm (0.018 in) Diameter Via Hole

Immersion tin is a suitable minimum risk selection that has been successfully used by some companies in below gigahertz frequency applications. It is a potentially viable lead-free finish option for some PCB applications.

From a mitigation viewpoint, there are several options that should be reviewed if assembling a PWB with an Immersion Tin surface finish. The first option should be to ensure that all surfaces plated with tin be soldered, including vias. The consumption of the deposit as a function of soldering will all but eliminate any potential for whisker growth [57]. Where it is not possible to solder all vias, the use of hole-fill materials should be investigated. For vias used as test points, the use of conductive hole-fill material that is subsequently plated over with copper/immersion tin (considered at this stage a round SMT pad) and then soldered, will help mitigate whisker formation but still provide test point capability.

5.10.2 Non-Tin Lead-free PCB Finishes

For over 15 years, the PCB industry has offered many alternate surface finishes that were developed in response to technology demands. The majority of these finishes are lead free which makes them ideally suited for compliance to the European Directives (WEEE, RoHS). The majority of the alternate surface finishes do not contain Tin. Unlike some of the alternatives proposed for lead frame and component finishes, these alternatives are cost effective and in some cases may even be cheaper than current Tin/Lead or Immersion Tin. A list of Lead Free / Tin free surface finishes available includes:

1) OSP (Organic Solderability Preservatives)
2) Immersion Silver
3) ENIG (Electroless Nickel/Immersion Gold)
4) Electroless Palladium
5) Universal finish – Nickel/Palladium/Gold
6) DIG – Direct Immersion Gold over copper (no nickel barrier)

It should be noted that each of the non-tin options has its own idiosyncrasies that need to be addressed in each specific application.

5.10 Printed Circuit Board (PCB) and other component finishes (cont'd)

5.10.3 PCB Pretinning

HASL and wave solder are both processes for applying molten solder to the unassembled, non-populated PCB. Lead-free options are currently being explored.

6 Summary

A range of basic information on Sn whisker formation and some current mitigation practices have been described in this document. For more information on these various aspects, one should refer to the bibliography found in Annex B for relevant articles on these subjects. As new studies on Sn whisker formation and mitigation are completed, this document will be updated to reflect those findings.

Annex A (informative) List of References

[1] Tin (and Other Metal) Whisker Induced Failures, NASA Goddard Space Flight Center http://nepp.nasa.gov/whisker/failures/index.htm

[2] S.E. Koonce and S.M. Arnold, "Metal Whiskers", J. Appl. Phys. (letters to the editor), 25(1): pp. 134-135, 1954

[3] H. P. Kehrer and H.G. Kadereit, "Tracer Experiments on the Growth of Tin Whiskers", Applied Physics Letters, 16(11): pp 411-412, June 1970.

[4] R.M. Fisher, L.S. Darken, and K.G. Carroll, "Accelerated Growth of Tin Whiskers", Acta Metallurgica. 2(3): pp. 368-372, May 1954 .

[5] K.G. Compton, A. Mendizza, and S.M. Arnold, "Filamentary Growths on Metal Surfaces Whiskers," Corrosion 7: pp. 327-334, 1951.

[6] S.M. Arnold, "The Growth of Metal Whiskers on Electrical Components", Proc. of the IEEE Elec. Comp. Conf., pp. 75-82, 1959

[7] GEB-0002, "Reducing the Risk of Tin Whisker-Induced Failures in Electronic Systems".

[8] George T. Gaylon, "Annotated Tin Whisker Bibliography and Anthology", IEEE Transactions on Electronics Packaging Manufacturing, 28(1): pp. 94-122, January 2005.

[9] J.W. Osenbach, J.M. DeLucca, B.D. Potteiger, R.L. Shook and F.A. Biaocchi, "Sn Corrosion and It's Influence on Whiskers", The ECTC iNEMI Tin Workshop, Orlando, FL, June 1, 2005.

[10] H. L. Reynolds and r. Hilty, "Investigation of Zinc Whiskers using FIB Technology", IPC/ JEDEC Lead (Pb) Free Conference, Boston, MA, Dec. 3, 2004.

[11] K.G. Compton, A. Mendizza, and S.M. Arnold, "Filamentary Growths on Metal Surfaces - "Whiskers," *Corrosion* 7(10): pp. 327-334, October 1951.

[12] Jie-Hua Zhao, Peng Su, Min Ding, Sheila Chopin, and Paul S. Ho, "Microstructure-based Stress Modeling of Tin Whisker Growth", Proceedings of the 55th ECTC

[13] G. T. Galyon, C. Xu, S. Lal, B. Notohardjono, The 2nd iNEMI Tin Workshop, Orlando, FL, May 31, 2005.

[14] B.Z. Lee and D.N. Lee, "Spontaneous Growth Mechanism of tin Whiskers", Acta Metallurgica, 46(10): pp. 3701-3714, 1998.

[15] S. Madra, "Thermo-Mechanical Characterization of Lead-Free Tin Plating: X-ray Diffraction Measurements and Correlation with Analytical and Numerical Models", IPC/ JEDEC Meeting, Frankfort, Germany, October 11, 2003.

Annex A (informative) List of References (cont'd)

[16] Peng Su, Jim Howell, and Sheila Chopin, "A Statistical Study of Sn Whisker Population and Growth during Elevated Temperature and Humidity Storage Tests",
55th ECTC Workshop

[17] Peng Su, Min Ding, and Sheila Chopin, "Effects of Reflow on the Microstructure and Whisker Growth Propensity of Sn Finish", Proceedings of the 55th ECTC

[18] J. Smetana, "Theory of Tin Whiskers", IEEE CPMT Transactions, April 2006 and 2nd iNEMI Tin Workshop, Orlando, FL, May 31, 2005.

[19] Wan Zhang, Andre Egli, Felix Schwager, and Neil Brown, "Investigation of Sn–Cu Intermetallic Compounds by AFM: New Aspects of the Role of Intermetallic Compounds in Whisker Formation", IEEE Transactions on Electronic Packaging Manufacturing, 28(1), January 2005.

[20] M. Dittes, P. Oberndorff, P. Crema, V. Schroeder, "Tin Whisker Formation in Thermal Cycling Conditions", Proc. Of 5th Electronics Packaging Technology Conference (EPTC), December 2003, Singapore, pp 183 – 188.

[21] George T. Galyon and l. Palmer, "An Integrated Theory of Whisker Formation: The Physical Metallurgy of Whisker Formation and the Role of Internal Stresses", IEEE Transactions on Electronic Packaging Manufacturing, 28(1): pp. 17-30, January 2005.

[22] Keith Sweatman, Shoichi Suenaga and Tetsuro Nishimura, "Suppression of Tin Pest in Lead Free Solders", Nihon Superior Co., Ltd., IPC/JEDEC 8th International Conference on Lead-Free Electronic Components and Assemblies, San Jose, CA, April 18-20, 2005

[23] A. Egli. W. Zhang, J. Heber, F. Schwater and M. Toben, "Where Crystal Planes Meet: Contribution to the Understanding of Whisker Growth Process", IPC Annual Meeting, pp. S8-3-1 – S-8-3-5, Nov. 2002.

[24] W.J. Boettinger, C.E. Johnson, L.A. Bendersky, K.W. Moon, M.E. Williams, G.R. Stafford, "Whisker & Hillock Formation on Sn, Sn-Cu and Sn-Pb Electrodeposits", submitted to Acta Met. (March 2005).

[25] M. W. Barsoum, E. N. Hoffman, R. D. Doherty, S. Gupta and A. Zavaliangos, "Driving Force and Mechanism for Spontaneous Metal Whisker Formation", Physical Review Letters, 93(20), pp. 206104-1 to 206104-4, Nov. 12, 2004.

[26] K.N. Tu, "Irreversible Processes of Spontaneous Whisker Growth in Bimetallic Cu-Sn Thin Reactions", Phys. Rev. B, 49(3): pp. 2030-2034, January 1994.
[27] J. Osenbach, R. Shook, B. Vaccaro, B. Potteiger, A. Amin, and P. Ruengsinub," "Lead Free Packaging and Sn-Whiskers," 54th Electronic Components and Technology Conference, pp. 1314-1324, 2004.

[28] W. J. Choi, T. Y. Lee, K. N. Tu, N. Tamura, R. S. Celestre, A. A. MacDowell, Y. Y. Bong, L. Nguyen, and G. T. T. Sheng, "Structure and Kinetics of Sn Whisker Growth on Pb-free Solder Finish," 52nd Electronic Component & Technology Conference Proceedings (IEEE Catalog number 02CH3734-5), San Diego, CA, 628-633 (2002).

Annex A (informative) List of References (cont'd)

[29] S. C. Park and D. C. Abbott, "Nickel-Palladium Based Component Terminal Finishes", HDP User Group International, Inc., http://www.hdpug.org/public/4-papers/2005/finishes/ppf-final-report-ver2.pdf

[30] Telcordia GR78-Core, Issue 1, September 1997, "Physical Design and Manufacture of Telecommunuications Products.

[31] S. M. Arnold, "The Growth of Metal Whiskers on Electrical Components", Proc. Of IEEE ECC, pp. 75-82, 1959.

[32] V.K. Glazunova and N.T. Kudryavtsev, "An Investigation of the Conditions of Spontaneous Growth of Filiform Crystals on Electrolytic Coatings", translated from Zhurnal Prikladnoi Khimii, 36(3): pp. 543-550, March 1963.

[33] G.J. Ewell, and F. Moore, "Tin Whiskers and Passive Components: A Review of the Concerns", Proc. of the 18th Conference on Capacitor and Resistor Technology", CARTS: pp. 222-228, March 1998.

[34] I. Yanada, "Electroplating of Lead-Free Solder Alloys Composed of Sn-Bi and Sn-Ag", Proc. Of the IPC Printed Circuits Expo, Long Beach USA: pp. S11-2 to S11-2- 7, April 1998.

[35] D. Hillman, "JCAA/ JG-PP No-Lead Solder Project: -20 C to +80 C & -55 C to +125 C Thermal Cycle Testing", SMTA International Conference Proceedings, 2005, pp. 846-850.

[36] J. Bradford, J. Felty and B. Russell, JCAA/ JG-PP No-Lead Solder Project: Combined Environments Test", SMTA International Conference Proceedings, 2005, pp. 824-840.

[37] M. Dittes, P.Oberndorff and L.Petit, "Tin Whisker Formation – Results, Test Methods and Countermeasures" Proc. 53rd. Electronic Components & Technology Conference 2003, pp. 822-826

[38] J.W. Osenbach, R.L. Shook, B.T. Vaccaro, A. Amin, B.D. Potteiger, K.N. Hooghan, P. Suratkar, and P. Ruengsinsub, "Tin Whisker Mitigation: Application of Post Mold Nickel Underplate on Copper Based Lead Frames and Effects of Board Assembly Reflow", Proceedings Surface Mount Technology Assoc., 2004, pp. 724-734.

[39] W.K. Choi, S.K. Kang, Y.C. Sohn and D.Y. Shih, "Study of IMC Morphologies and Phase Characteristics Affected by the Reactions of Ni and Cu Metallurgies with Pb-Free Solder Joints", Electronic Components and Technology Conference, pp. 1190-1196, 2003.

[40] Oberndorff, P.J.T.L; Dittes, M; Petit, L; "Intermetallic Formation in Relation to Tin Whiskers" Proc. of the IPC/ Soldertec International Conference "Towards Implementation of the RHS Directive" June, 11-12 2003, Brussels, Belgium, pp. 170-178

[41] V.K. Glazunova and N.T. Kudryavtsev, "An Investigation of the Conditions of Spontaneous Growth of Filiform Crystals on Electrolytic Coatings", translated from *Zhurnal Prikladnoi Khimii*, 36(3): pp. 543-550, March 1963.

Annex A (informative) List of References (cont'd)

[42] J. Osenbach, R. Shook, B. Vaccaro, B. Pottieger, A. Amin, P. Ruengsinsub, and K. Hooghan, "The Effects of Board Assembly Reflow Processing on Sn Whisker Formation," Proc. IPC/JEDEC Pb-Free Conference, Mar. 2004.

[43] B. Rickett, G. Flowers, S. Gale and J. Suhling, "Potential for Whisker Formation in Lead-Free Electoplated Connector Finishes", Proceedings SMTA International Conference, Chicago, IL, Sept. 2004, pp 707-716.

[44] Oberndorff P., Dittes M., Crema P., "Whisker Formation on Sn Plating" Proc. IPC / JEDEC 5th Intern. Conference on Pb-Free Electronic Assemblies and Components, March 2004, San José, USA

[45] Qualification Test Report of Tin Whisker, ERCS05-002, January 21, 2005
Development Department, NEC TOKIN Iwate, Ltd.

[46] NEMI DOE 3 – presented at ECTC 2005, Valeska Schroeder et. Al. To be published IEEE CPMT Transactions April 2006

[47] John W. Osenbach, Richard L. Shook, Brian T. Vaccaro, Brian D. Potteiger, Ahmed N. Amin, K. N. Hooghan, P. Suratkar, and P. Ruengsinsub, "Sn Whiskers: Material, Design, Processing, and Post-Plate Reflow Effects and Development of an Overall Phenomenological Theory", IEEE Transactions on Electronic Packaging Manufacturing, 28(1), January 2005.

[48] R. Schetty, N. Brown, A. Egli, J. Heber and A. Vinckler, "Lead-Free Finishes- Whisker Studies and Practical Methods for Minimizing the Risk of Whisker Growth", Proc. Of AESF SUR/FIN Conf., pp. 1-5, June 2001.

[49] Thomas A. Woodrow and Eugene A. Ledbury, "Evaluation of Conformal Coatings as a Tin Whisker Mitigation Strategy", IPC/JEDEC 8th International Conference on Lead-Free Electronic Components and Assemblies, San Jose, CA, April 18-20, 2005.

[50] Jong Kadesch and Jay Brusse, "The Continuing Dangers of Tin Whiskers and Attempts to Control Them with Conformal Coating", NASA's EEE Links Newsletter, July 2001.
http://nepp.nasa.gov/whisker/index.html

[51] B. Hilty, N. Corman, F. Herrmann, Electrostatic Fields and Current Flow Impact on Whisker Growth, IEEE Transactions on Electronic Packaging Manufacturing, 28(1), January 2005.

[52] D. Romm, D. Abbott, S. Grenney, and M. Khan, "Whisker Evaluation of Tin-Plated Logic Component Leads, Texas Instruments Application Report SZZA037A, pp. 1- 27, February 2003.

[53] P. Oberndorff, M. Dittes, P. Crema, "Whisker Testing: Reality and Fiction", Electronics, June 2004, Amsterdam, The Netherlands.

[54] Ki-Hwan Park et. al., "Reliability of SnBi Lead Finished Lead-Free Product", 2002 International Symposium on Electronic Materials and Packaging.

[55] Solder Joint Reliability SnBi lead finishes – NEC web site
http://www.necel.com/pkg/en/pb_free/images/F0706_l.gif

Annex A (informative) List of References (cont'd)

[56] J. Lau and Y. Pao, "Solder Joint Reliability of BGA, CSP, Flip Chip and Fine Pitch SMT Assemblies", McGraw Hill, ISBN 0-07-036648-9.

[57] Draft IPC-4554, "Specification for Immersion Tin Plating for Printed Circuit Boards", 2005 by the IPC 4-14 Plating Process Subcommittee.

Annex B Bibliography

[1] Lau, J. H., and K. Liu, "Update of Global Trends in Lead-Free Soldering", Proceedings of SMTA International Conference, Chicago, Il, September 2004, pp. 810-830.

[2] Lau, J. H., and S. Pan, "3D Nonlinear Stress Analysis of Tin Whisker Initiation on Lead-Free Components", ASME Transactions, Journal of Electronic Packaging, Vol. 125, December 2003, pp. 621-624.

[3] Lau, J. H., S. Pan, and C. Xu, "3D Large Deformation and Nonlinear Stress Analysis of Tin Whisker Initiation and Growth on Lead-Free Components", IEEE Proceedings of Electronic Components & Technology Conference, May 2003, pp. 692-697.

[4] **IEEE Transaction on Electronics, Packaging and Manufacturing**, January 2005. **Special Issue on Tin Whiskers**

[4a] Vo, M. Kwoka, and P. Bush , "Tin Whisker Test Standardization", IEEE Transactions on Electronic Packaging Manufacturing, 28(1), January 2005.

[4b] I. Sakamoto ,"Whisker Test Methods of JEITA Whisker Growth Mechanism for Test Methods", IEEE Transactions on Electronic Packaging Manufacturing, 28(1), January 2005.

[4c] C. Xu, Y. Zhang, C. Fan, and J. A. Abys, "Driving Force for the Formation of Sn Whiskers: Compressive Stress—Pathways for Its Generation and Remedies for Its Elimination and Minimization", IEEE Transactions on Electronic Packaging Manufacturing, 28(1), January 2005.

[4d] S. Lal and T. D. Moyer, "Role of Intrinsic Stresses in the Phenomena of Tin Whiskers in Electrical Connectors", IEEE Transactions on Electronic Packaging Manufacturing, 28(1), January 2005.

[5] "Avoiding Tin Whisker Reliability Problems", G.T. Galyon & Ron Gedney, Circuits Assembly, August 2004, pp 26-31.

[6] J. Smetana, "Theory of Sn Whiskers", IEEE CPMT, April 2006.

[7] Jie-Hua Zhao, Peng Su, Min Ding, Sheila Chopin. And Paul S. Ho, "Microstructure-based Stress Modeling of tin Whisker Growth", Proceedings 55th ECTC.

[8] Peng Su, Min Ding, and Sheila Chopin, "Effects of Reflow on the Microstructure and Whisker Growth Propensity of Sn Finish", Proceedings of the 55th ECTC, pp 434-440., 2005.

[9] M. Dittes, Infineon "Humidity Effects on Sn Whisker Formation", iNEMI Tin Whisker Workshop at ECTC, Orlando, 2005.

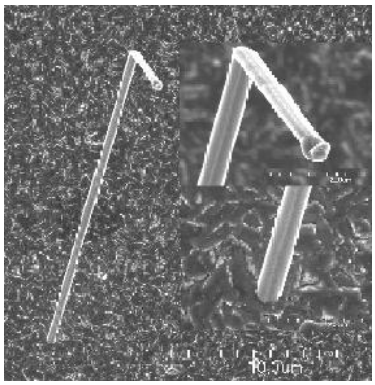
[10] Peng Su, "A statistical Study of Sn Whisker Population & Growth During Elevated Temperature/Humidity Storage Test", iNEMI Tin Whisker Workshop at ECTC, Orlando, 2005.

[11] J. Osenbach, "Sn Corrosion and Its Influence on Whiskers", iNEMI Tin Whisker Workshop at ECTC, Orlando, 2005.

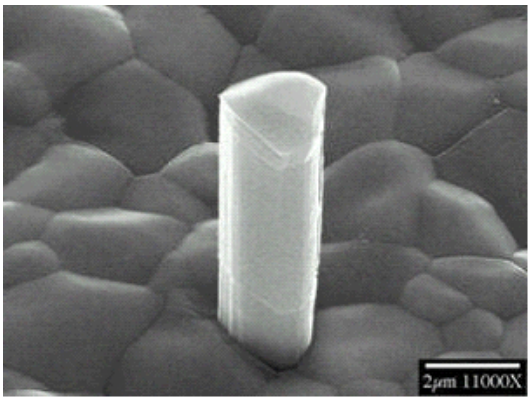
[12] P. Oberndorff, M. Dittes, P. Crema, S. Chopin, "Whisker Formation on Matte Sn Influencing of High Humidity", 2005 Electronic Component and Technology Conference, pp 429-433, Orlando.

Annex C Tin Whisker Images

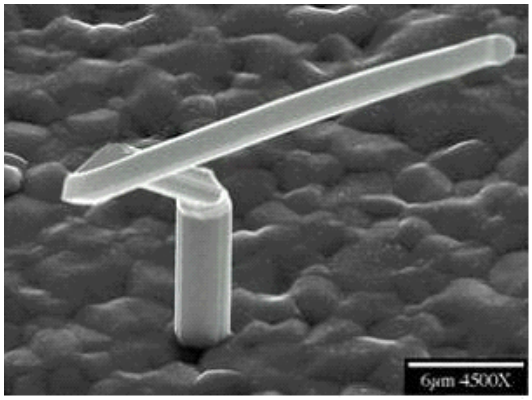
A collection of scanning electron microscope images are presented in the annex that exemplifies the appearance of tin whiskers.



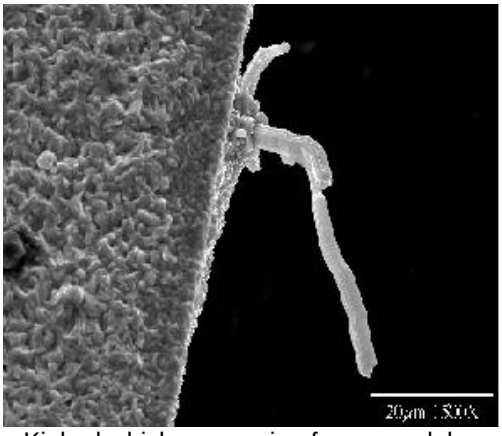
Tin whisker filaments.



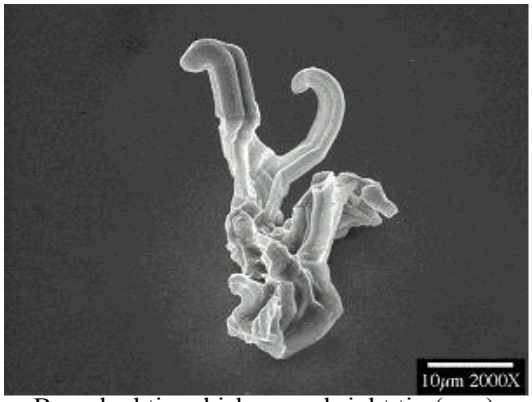
Whisker with a consistent cross section.



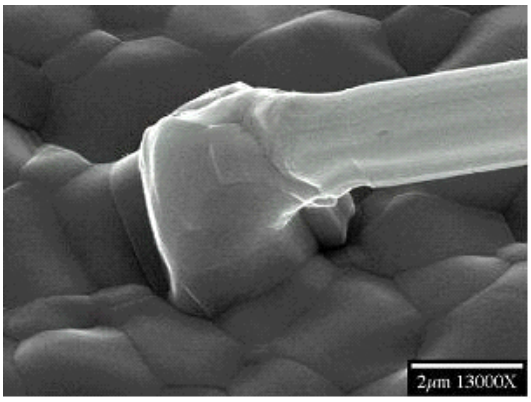
Kinked whisker.



Kinked whiskers growing from a nodule.

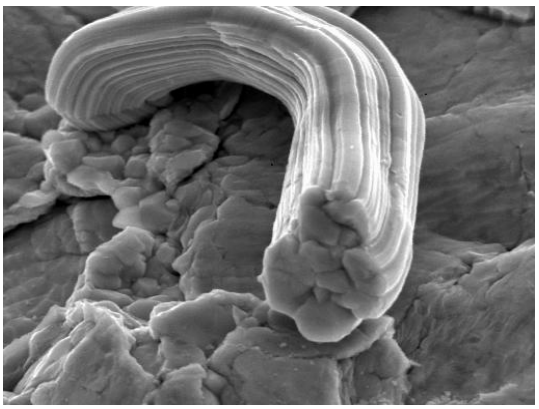


Branched tin whiskers on bright tin (rare).

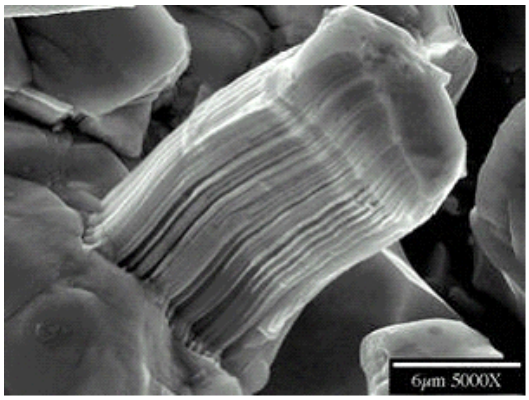


Whisker initiating from a hillock.

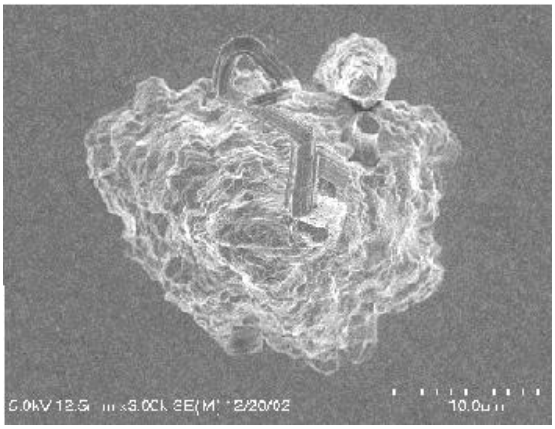
Annex C Tin Whisker Images (cont'd)



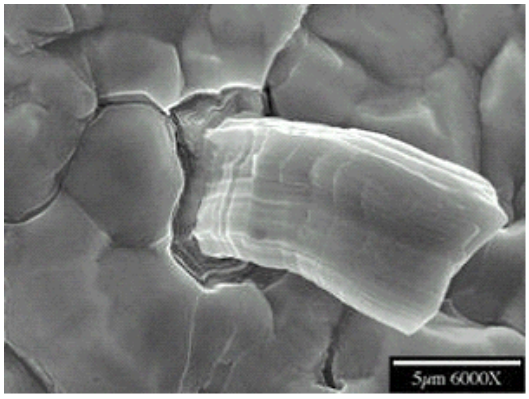
Tin whisker filament with striations.



Tin whisker filament with striations.



Kinked whisker on odd-shaped eruptions.



Tin whisker with rings.

Standard Improvement Form *JEDEC/IPC JP002*

The purpose of this form is to provide the Technical Committees of IPC and JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to IPC and JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to both associations:

IPC, Association Connecting Electronics Industries
3000 Lakeside Drive
Bannockburn, IL 60015
Fax: 847.615.5693

JEDEC
2500 Wilson Blvd.
Arlington, VA 22201-3834
Fax: 703.907.7583

1. I recommend changes to the following:

   _____ Requirement, paragraph number _____

   _____ Test method number _____ Paragraph number _____

   The referenced paragraph number has proven to be:

   _____ Unclear _____ Too Rigid _____ In Error

   _____ Other _____

2. Recommendations for correction:

3. Other suggestions for document improvement:

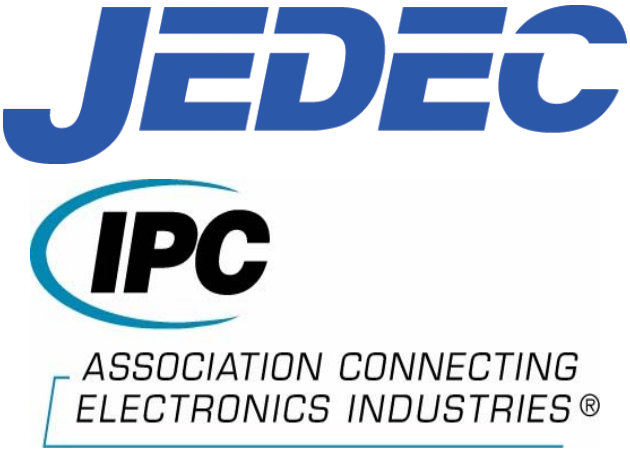
Submitted by:

Name: Telephone:

Company: E-mail:

Address:

City/State/Zip: Date:


JEDEC
IPC
ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES®